CALYPTO | Catapult Product Family Datasheet

KEY BENEFITS

- Native SystemC and ANSI C++ synthesis
- Write 80% less code
- Simulate 100-1000x faster
- Explore microarchitecture alternatives
- RTL optimized for power, performance, area, and RTL verification
- Simplified RTL functional coverage closure
- Mix datapath and control logic synthesis
- Top-down and bottom-up hierarchical design management
- Full control over design interfaces
- Incremental synthesis constraints for ECO

ACCELERATE TIME TO RTL, REDUCE VERIFICATION COST

Traditional hardware design methods require manual RTL development and debugging, which are time consuming and error prone. The Catapult® high-level synthesis tool empowers designers to use abstract synthesizable designs, which typically require 80% less hand-written code and simulate up to 1000x faster than synthesizable RTL . From these high-level descriptions Catapult generates optimized RTL ready for production RTL synthesis and verification flows.

Catapult's unified flow for modeling, synthesizing, and verifying complex ASICs and FPGAs allows expensive coverage simulations to be developed much more quickly using the abstract source. For example, a coverage simulation that runs overnight on 100 CPUs could run in less than an hour on a single machine. The highly interactive Catapult workflow provides full visibility and control of the synthesis process, enabling designers to rapidly design and verify the best implementation for performance, area, and power. Catapult then generates Verilog or VHDL RTL, constraints files for RTL synthesis and a wrapper that allows the C++ or SystemC test environment to be re-used.

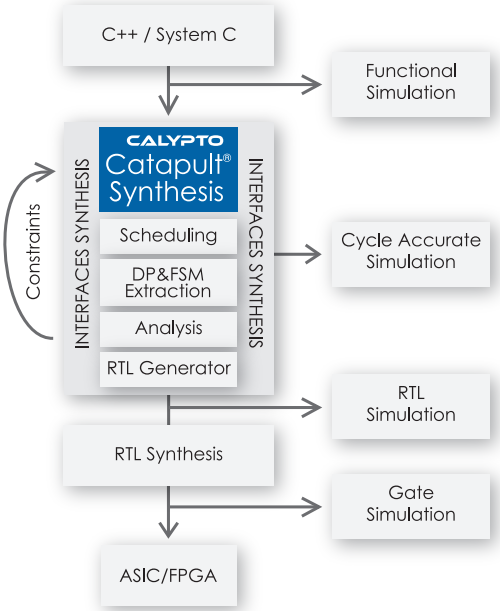
KEY DIFFERENTIATORS

Native SystemC and ANSI C++ Synthesis

The Catapult offers native support both for pure untimed ANSI C++ and for SystemC, without the need to write wrappers or adaptors. This allows each design team to select the language that best meets the needs of their current project and to switch languages in the future if their needs change.

Hierarchy Synthesis

Catapult synthesizes multi-block pipelined and concurrent hierarchical designs from pure sequential ANSI C++ and SystemC.



Front-to-Back, Fully Automated Verification

Catapult integrates a push-button, fully automated verification flow that produces all the required files and scripts to verify a generated design. This allows verification teams to focus on the SystemC or C++ source and reduces the cost of verification. Both functional simulation and formal methods for verification are integrated with Catapult.

Micro-Architecture Analysis and Optimization

Catapult combines automation with specific high-level constraints so designers can precisely control the hardware implementation and converge on the optimal mirco-architecture for power, performance, and area.

Interface Synthesis

Catapult accepts pure ANSI C++ description as its input and uses patented interface synthesis technology to control the timing and communications protocol on the design interface, so designers can can explore a full range of hardware interface options without changing the source.

SystemC Modular IO

Catapult synthesizes abstract SystemC transaction models as well as lower abstraction cycle accurate models. Leveraging Catapult Modular IO library, customers can easily specify point-to-point block interconnect without degrading simulation speed or hardware quality. The standard interconnect includes point-to-point handshake, FIFO and memories. Catapult also supports custom IO written in standard SystemC and can even support complex bus interfaces. Modular IO libraries simplify writing, debugging and integrating designs by giving a consistent way to define and use interfaces.

Low-Power Exploration and Optimization

Catapult LP (low power) takes advantage of Calypto's leading PowerPro technology under the hood to seamlessly produce the lowest power RTL and deliver up to 80% power savings at the architectural level. Starting with SystemC or C++, Catapult LP performs power estimation, architectural power optimizations and fine grain sequential clock gating. With Catapult LP designers can explore different hardware architectures, including various memory banking schemes, to produce the ultimate in low power hardware designs.

Synthesis, Verification and ECO Flows

Calypto's offers an integrated ESL design flow which tightly couples Catapult for high level synthesis with SLEC for sequential formal equivalence checking. The flow dramatically reduces time to design and verify hardware subsystems. Calypto's ESL design flow connects SystemC TLM 2.0 virtual platforms, system verification and emulation by partnering with Mentor and other EDA providers. After more than 1000+ ASIC tapeouts, Catapult has proven integration with DesignCompiler for predictable timing closure and Conformal ECO for engineering change orders.

Predictable Timing Closure

Catapult features technology-aware scheduling and allocation heuristics to produce superior designs and predictable timing closure in the physical design stage.

CATAPULT PRODUCT FAMILY

Feature	CALYPTO Catapult® SL	CALYPTO Catapult® LP
C++	√	√
SystemC	√	√
Multi-million gate designs	√	√
Bottom-up Synthesis	√	√
Optimizes Algorithms	√	√
Optimizes Control Logic	√	√
Optimizes for RTL Coverage	√	√
Power efficient stall logic	√	√
Integrated RTL Power Analysis		√
Vectorless clock gating		√
Vector based sequential clock gating		√
Generates VHDL and Verilog	√	√
Re-use C++/SystemC testbench on RTL	√	√

SYSTEM REQUIREMENTS AND COMPATIBILITY

Languages: VHDL 87, 93 & 97 and Verilog 95 & 2001, SystemVerilog
Platforms: Windows 7, Linux Red Hat Enterprise 5 and 6
Memory: 2 GB minimum

calypto.com

World Headquarters	Calypto Europe	Calypto India	Calypto Japan	Calypto China	Calypto Korea	Calypto Israel
Tel: +1.408.850.2300	Tel: +44.776.5800.801	Tel: +91 120 472.1600	Tel: +81.45.470.2070	+86.10.6805.8081	Tel: +82.2.488.3538	Tel: +972.54.833.4451
info_na@calypto.com	info_eu@calypto.com	info_in@calypto.com	info_jp@calypto.com	info_cn@calypto.com	info_kr@calypto.com	info_il@calypto.com